Proc. of Int. Conf. on Advances in Power Electronics and Instrumentation Engineering, PEIE

Selective Harmonic Elimination of Three Phase Bidirectional AC Buck Converter for Power Quality Improvement

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***Abstract*— A novel three phase bidirectional AC buck converter circuit using power MOSFET is analyzed for input power factor, harmonic profile and efficiency of the converter for power quality improvement. The equal PWM (EPWM) technique is a used to increase number of pulses per half cycle (P) in order to vary these parameters. The rms value of the fundamental component of the output voltage can be increased by varying the duty ratio (K) of the pulses. It is observed from the simulation results obtained using MATLAB/simulink that the proposed scheme using EPWM technique significantly reduces low order harmonics, eliminates certain harmonics for certain values of P, improves input power factor and hence significantly reduces the filter size of the converter.**

***Index Terms*— Three phase AC chopper, AC snubbers, Harmonic Profile, Equal PWM, Power quality.**

I. INTRODUCTION

Industrial loads such as heaters, illumination control, furnaces, AC motor speed control and also theatre dimmers uses AC voltage controllers. Such voltage regulators, however, have slow response, poor input power factor and high magnitude of low order harmonic at both input and output sides. These converters need large input-output filters to reduce low order harmonics in the line current. These drawbacks have been overcome by designing various topologies of AC chopper [1-7]. In most standard AC choppers, the commutation causes high voltage spikes and an alternative current path has to be provided when current paths are changed. This alternative current path is implemented using additional bidirectional switches. Such topologies are difficult and expensive to realize and the voltage stress of the switch is also high, resulting in reduced reliability.

Fig.1 shows the block diagram of three phase AC buck chopper with control circuit to generate pulses to power MOSFET embedded four quadrant switches operating in high frequency chopping mode. In this paper, a novel bidirectional three phase AC buck converter is proposed and analysed for R load using EPWM technique where number of pulses per half cycle (P) is increased in order to change the harmonic profile of the output voltage and input source current. The power circuit is made up of a PWM buck chopper which

DOI: 02.PEIE.2014.5.20

uses three sets of four quadrant bidirectional switches with AC snubbers for each phase. The AC voltage chopper is controlled using EPWM pattern which is efficient and simple to implement.

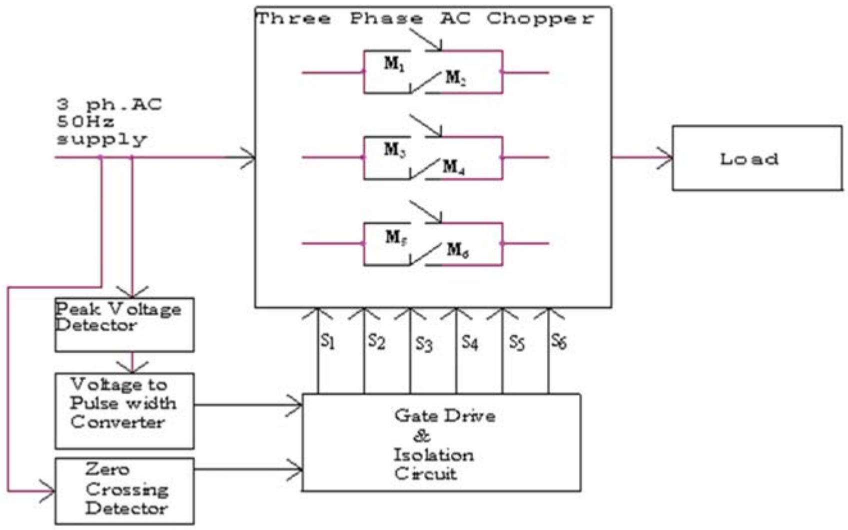

Fig. 1. Block Diagram of the proposed three phase buck AC Chopper

The control circuit comprises of saw tooth pulse generator of desired frequency which is compared with the variable DC voltage $V_{control}$ to generate switching pulses. The ZCD pulses are obtained by stepping down the three phase voltage and then passed through the zero crossing detectors. The PWM pulses and ZCD pulses are given to the six switches through logic circuit. The output voltage can be continuously varied by varying duty ratio (K) of the pulses. The technique continues to evoke interest with respect to variation of P and K [8]. The chopped output line voltage waveform is analysed for harmonic content for various values of P & K [9-10]. This technique can be adopted for the selective harmonic elimination and reduction at the high frequency chopping mode facilitating easy filtration at lower cost.

II. Description Of Three Phase Buck Ac Converter

Fig. 2 shows the three phase buck AC chopper with AC snubbers derived from the dc buck chopper, where the normal unidirectional switches are replaced with four quadrant bidirectional switches for each phase. The switches need series diodes to provide reverse blocking capability required in these converters. The important feature of the power MOSFETs that simplifies the gate drive circuit is its high input impedance. The switching speed of these switches is higher than IGBTs. They can withstand the simultaneous application of high current and high voltage (for a short duration) without undergoing destructive failure due to second breakdown. They can be easily paralleled as their forward voltage drop increases with increasing temperature. The control of the switches is based on the equal PWM technique. In practical realizations of the converter, stray inductances increase the voltage stress of the bidirectional switches and may destroy the switches. This situation requires the converter using AC snubber comprising RC combination (R_s and C_s) for each four quadrant switch of the three phases. The switching frequency of the switches is varied from 3.6 KHz (P=36) to 5.4 KHz (P=54) in order to observe the harmonic profile, input power factor and efficiency of the converter. The line voltage of 415 V with phase sequence ABC has been considered for evolving the switching states of the switches and simulating the converter.

III. Generation Of Gate Control Signal

Fig. 3 shows the block diagram of the control circuit. This circuit generates the PWM pattern gate control signals for six switches as that of the waveforms shown in the Fig. 7. The switching frequency is related to P and supply frequency f as

$$F_{sw} = 2Pf \qquad (1)$$

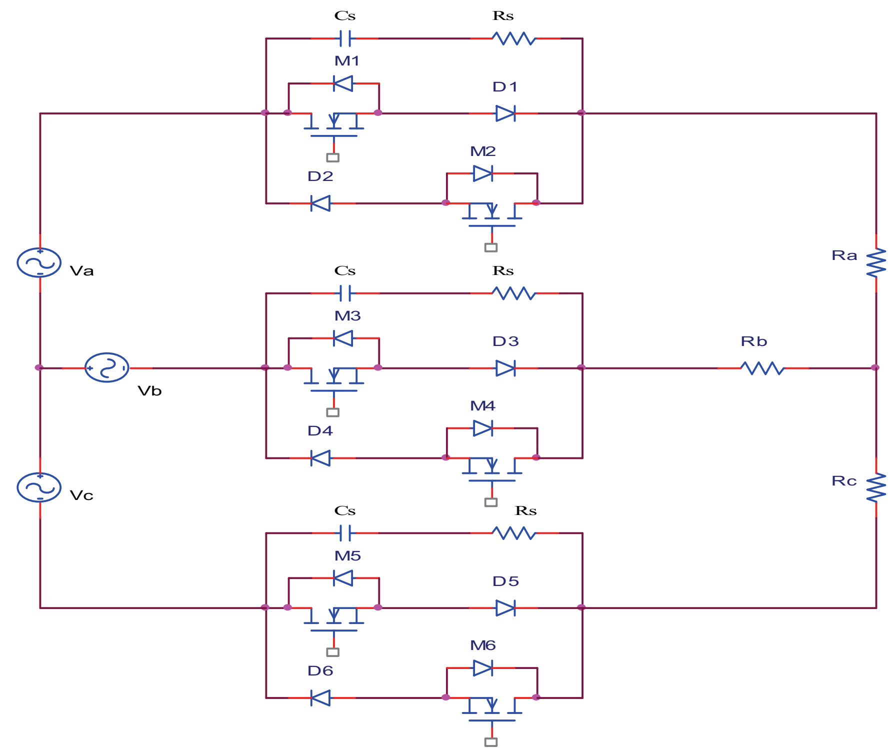

Fig.2 Three phase buck ac choppers using bidirectional switches and ac snubbers

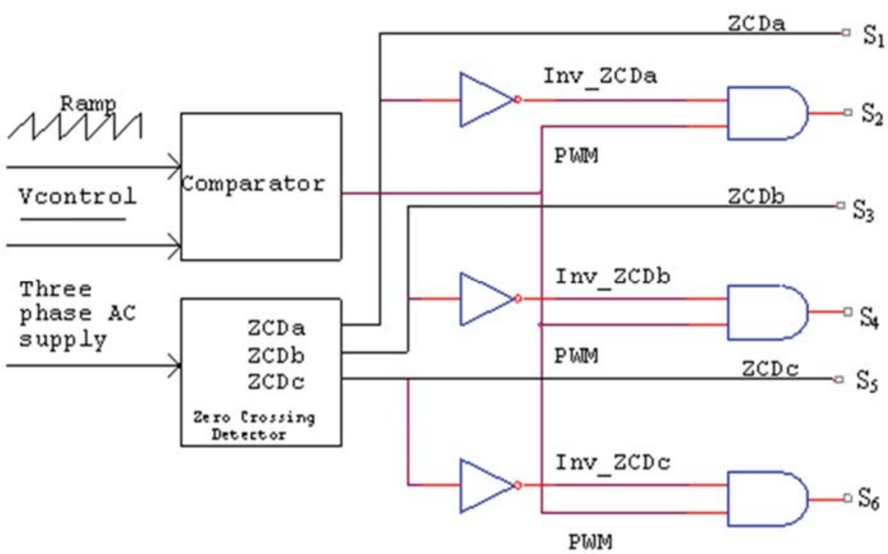

Fig. 3 Block Diagram of the control circuit to generate switching pulses

The EPWM pulses to be given to MOSFET switches are generated by comparing Ramp with control voltage $V_{control}$. The value of P can be selected by varying the frequency of the RAMP carrier wave. The value of P is set for various carrier frequencies like 3.6 KHz, 4.2 KHz, 4.8 KHz and 5.4 KHz to obtain the corresponding switching pulses. The value of the duty ratio K for every switching frequency can be varied by varying the control voltage $V_{control}$. The value of K is varied from 0.4 to 0.9 in order to vary the rms value of the fundamental component of the output voltage. The values of both P and K are varied in order to analyze the parameters like input power factor, Harmonic profile and efficiency of the converter.

IV. SIMULATION OF THE THREE PHASE BUCK AC CHOPPER

The Harmonic profile, input power factor and efficiency of the converter are investigated using MATLAB/simulink three phase buck AC chopper simulation model as shown in Fig. 4. The system characteristics are line voltage V_L= 415 V, semiconductor element MOSFET IRFPE40, snubber elements Rs=1.2KΩ & Cs=0.01μF, load parameters are R_o=529Ω per phase. The Switching frequency is varied from 3.6 KHz to 5.4 KHz and corresponding P is varied from 36 to 54 which is related as given in (2).

$$M = \frac{F_s}{2F} \tag{2}$$

Where Fs is the switching frequency and F is the supply frequency in Hz.

The simulation results include the input power P_s, the rms value V_{rms} of supply voltage V_s and I_{rms} of the source current I_s. Hence, the PF is calculated using the general definition as given in (3).

$$PF = \frac{P_s}{s} = \frac{P_s}{V_{rms} I_{rms}}$$

$$= \frac{\frac{1}{T}\int_0^T v_s(t) i_s(t) dt}{\sqrt{\frac{1}{T}\int_0^T v^2{}_s(t) dt}\sqrt{\frac{1}{T}\int_0^T i^2{}_s(t) dt}} \tag{3}$$

Fig. 4 shows the simulation model to satisfy (3) in order to calculate the input power factor. The efficiency can also be calculated as

$$\eta = \frac{P_o}{P_s} = \frac{\frac{1}{T}\int_0^T v_o(t) i_o(t) dt}{\frac{1}{T}\int_0^T v_s(t) i_s(t) dt} \tag{4}$$

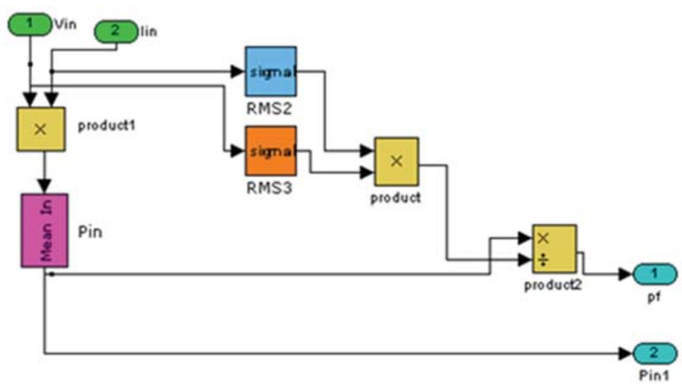

Fig. 4 Simulation model for PF calculation

The efficiency calculation as per equation (4) is modeled as one of sub model. The control circuit model compares saw tooth voltage with dc voltage to generate PWM pulses that are multiplied with three phase ZCD pulses ZCD_a, ZCD_b and ZCD_c to generate switching pulses for four quadrant switches of the converter.

Fig. 5 depicts the simulation model of three phase AC buck chopper having three sets of four quadrant switches with AC snubbers for each phase. The input side parameters like phase voltages, line currents are sensed to calculate input side rms values, input power factor and input power using sub models. Similarly output side parameters like output phase voltage and currents are sensed to calculate their rms values, output power and power factor that are load dependent by using sub models. Using all these parameters, the efficiency of the converter can be calculated as per equation (4) using sub models and displayed using numeric displays. Three phase AC voltage converter is capable of operation with inductive loads, however, the simulation is done for resistive load since harmonic currents are the worst in this case than that of RL loads.

The control circuit as shown in Fig. 6 consists of three ZCDs for each phase to convert the step down voltage of three phases to ZCD pulses. These ZCDs are basically relational operator that does the operation of

OPAMP circuits. The saw tooth carrier wave of amplitude 10V is compared with the DC control voltage that can be varied from 0 to 10V in order to adjust the duty ratio of the switching pulses from 0 to 1. The value of the variable P is varied by changing the frequency of the carrier saw tooth voltage waveform. The ZCD pulses ZCD_a, ZCD_b and ZCD_c are directly given to the switches M_1, M_3 and M_5 respectively. The inverted ZCD pulses of ZCD_a, ZCD_b and ZCD_c are ANDed with PWM pulses in order to give pulses to switches M_2, M_4 and M_6 respectively as shown in Fig. 7.

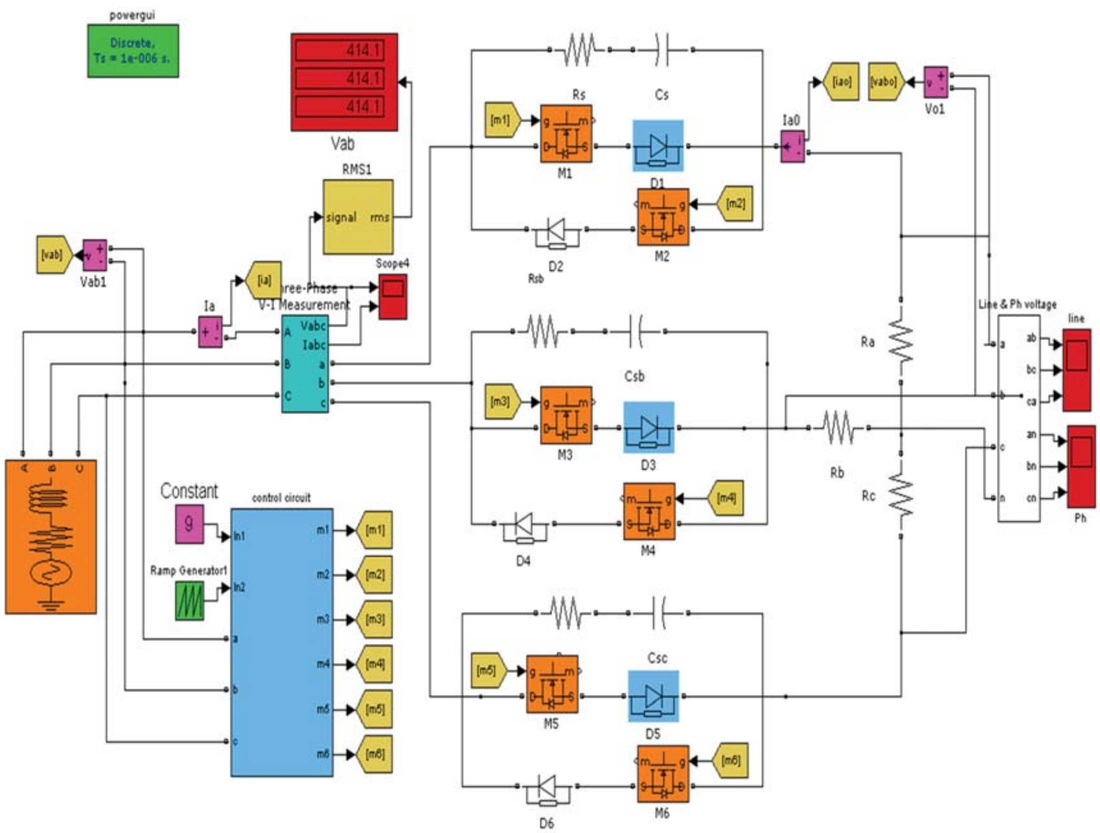

Fig.5 Three phase AC buck chopper simulation model

V. Simulation Results

The waveforms of the three phase output line voltages are shown in Fig.8. The peak value of the output line voltage is 587V i.e. √2time the rms value (415V) of the source line voltage. The line voltages have 36 pulses per half cycle corresponding to the gate pulses shown in Fig. 7. The output phase voltages are shown in Fig. 9. The peak value of the phase voltage is 338.9V i.e. 1/√3 times the peak value of the line voltage. It is observed that the chopped phase voltage has also 36 pulses per half cycle as that of line voltage waveforms. It is clear from the waveforms that the three phase voltages as well as the three line voltages are mutually displaced by 120^o.

Table I shows the variation of P & K and the corresponding converter parameters that include input power factor, total harmonic distortion of the source current and efficiency of the converter. It is observed form the table that with the increase in P from 36 to 54, the input power factor increases at the fixed duty ratio in each case. For instance, the input power factor is 0.5717 at P=36 and K=0.5. The input power factor has risen to 0.5805 at P=54 and K=0.5. The harmonic order up to 100^{th} order is considered for harmonic analysis in the simulation of the converter. The THD value of source current at K=0.5 is 84.66%, 83.86%, 83.38% and 1.93% corresponding to increasing values of P=36, 42, 48 and 54 respectively. The efficiency of the converter is increasing with the increase in the value of K from 0.4 to 0.9 at fixed frequencies.

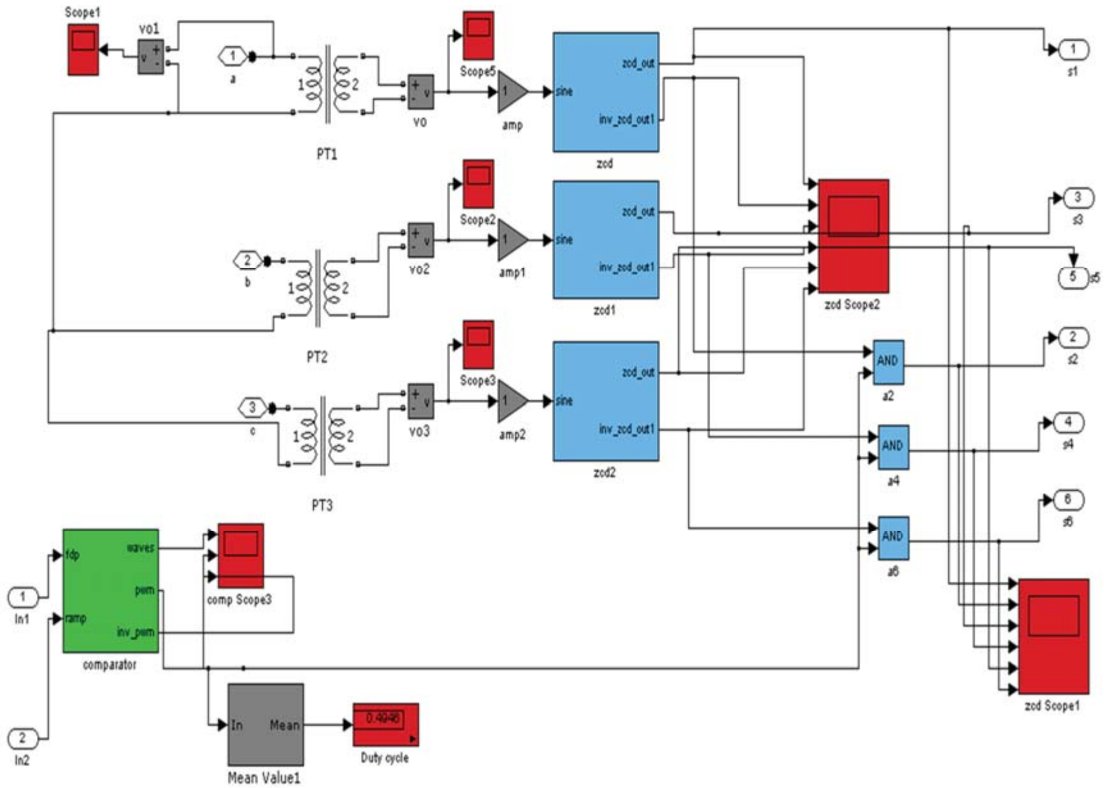

Fig.6 Simulation model of control circuit to generate switching pulses for MOSFET switches

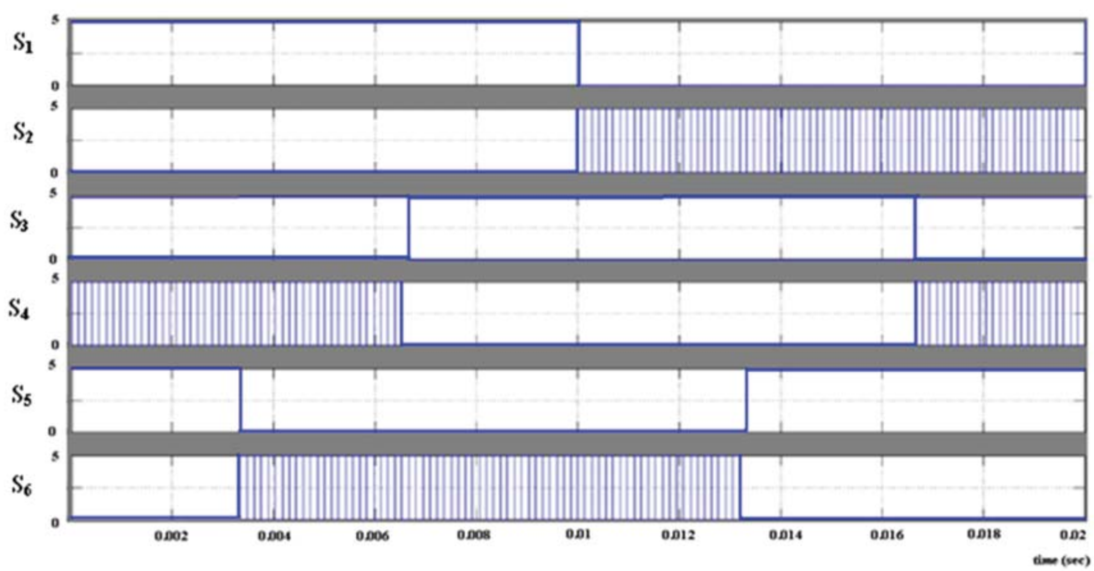

Fig.7 PWM pattern gate control signals for MOSFET switches

It is observed that with the increase in the value of P, there is small reduction in the efficiency at the fixed value of K due to more switching losses.

The harmonic components present in the source current are dependent on P as nP ±1. Where n is an even number. For instance, if P=36, then the order of the harmonic present are 2P ±1, 4P ±1 etc. In this way selective harmonic elimination can be done by selecting the proper value of P.

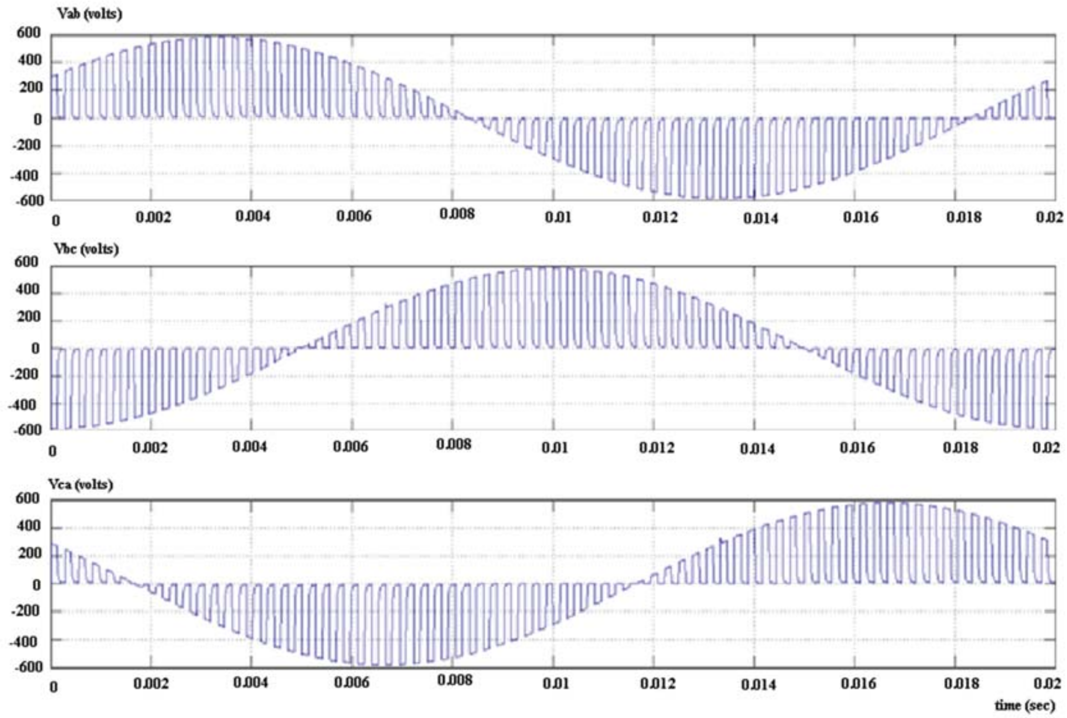

Fig. 8 Waveforms of the output line voltages for P=36 and K=0.5

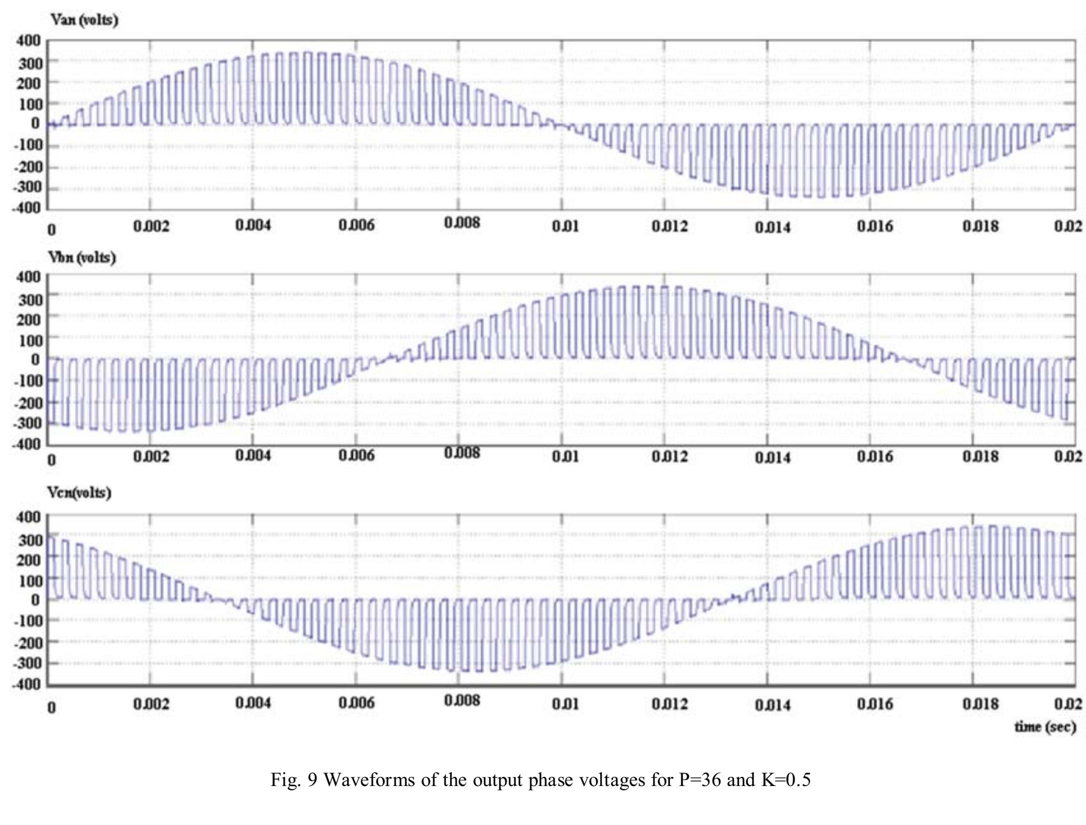

Fig. 9 Waveforms of the output phase voltages for P=36 and K=0.5

TABLE I. VARIATION OF P & K AND THE CORRESPONDING CONVERTER PARAMETERS

No. of pulses per half cycle (P)	Duty Cycle (K)	Output Voltage (Vab) volts	Output Current (Iao) Amps	Input Power Factor	Harmonic Components in %ge	THD (Is) in %ge	%η
36	0.4	260.7	0.2845	0.4972	Is71=70.93%, Is73=70.89%	100.32	94.84
	0.5	291.6	0.3182	0.5717	Is71=59.86%, Is73=59.82%	84.66	96
	0.6	319.5	0.3487	0.6486	Is71=47.42%, Is73=47.39%	67.07	96.8
	0.7	345.1	0.3767	0.73	Is71=34.42%, Is73=34.41%	48.62	97.39
	0.8	369	0.4028	0.8173	Is71=21.67%, Is73=21.58%	30.64	97.89
	0.9	391.4	0.4272	0.9099	Is71=9.96%, Is73=9.93%	14.08	98.46
42	0.4	260.6	0.2845	0.5003	Is83=70.41%, Is85=70.39%	99.59	94.41
	0.5	291.5	0.3182	0.5748	Is83=59.29%, Is85=70.89%	83.86	95.65
	0.6	319.4	0.3486	0.6518	Is83=47.06%, Is85=47.01%	66.56	96.5
	0.7	345.1	0.3766	0.733	Is83=34.17%, Is85=34.08%	48.32	97.15
	0.8	368.9	0.4027	0.8199	Is83=21.52%, Is85=21.49%	30.43	97.72
	0.9	391.3	0.4271	0.9111	Is83=9.93%, Is85=9.89%	14.04	98.39
48	0.4	260.4	0.2843	0.5031	Is95=69.83%, Is97=69.80%	98.77	93.98
	0.5	291.4	0.318	0.5777	Is95=58.95%, Is97=58.91%	83.38	95.3
	0.6	319.3	0.3485	0.6547	Is95=46.70%, Is97=46.65%	66.05	96.22
	0.7	345	0.3765	0.7359	Is95=33.91%, Is97=33.85%	57.96	96.93
	0.8	368.8	0.4026	0.8221	Is95=21.38%, Is97=21.31%	30.23	97.58
	0.9	391.2	0.427	0.912	Is95=9.91%, Is97=9.85%	14.01	98.33
54	0.4	260.3	0.2842	0.5059	All the Harmonic components up to 100th order all less than 2%	2.65	93.58
	0.5	291.3	0.3179	0.5805		1.93	94.97
	0.6	319.2	0.3484	0.6576		1.61	95.95
	0.7	344.9	0.3764	0.7385		1.36	96.73
	0.8	368.8	0.4025	0.8241		0.95	97.45
	0.9	391.1	0.4269	0.9127		0.61	98.27

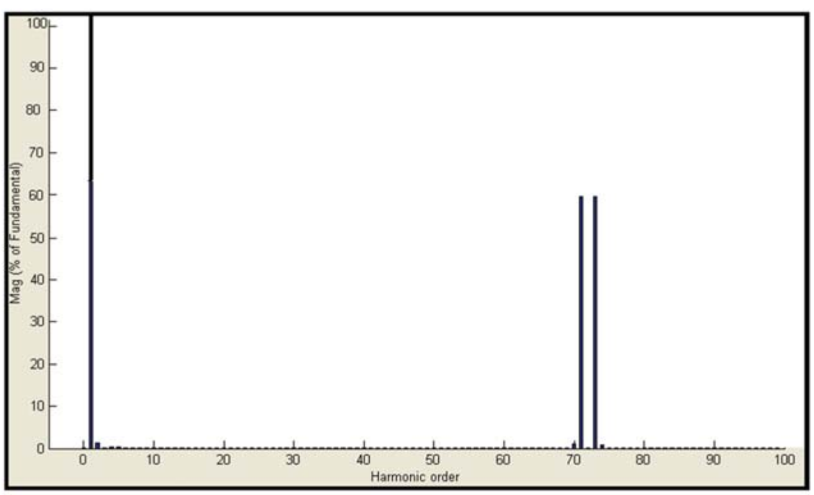

Fig. 10 FFT analysis of source current for P=36 and K=0.5

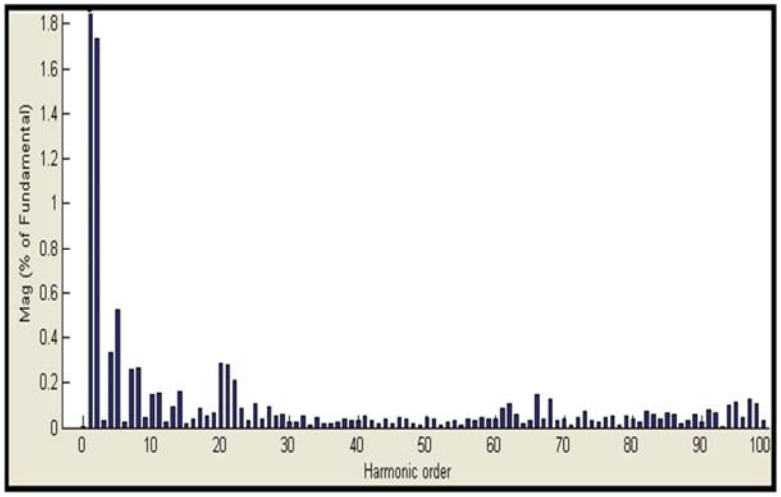

Fig. 11 FFT analysis of source current for P=54 and K=0.5

The FFT of the source current for P=36 and 54 at K=0.5 are shown in Fig. 10 and 11 respectively. The EPWM technique thus be employed selecting the P and K values for harmonic reduction and selective elimination, particularly those of the lower order that will facilitate design of the economical and smaller sized filters.

The main advantage of choosing higher switching frequency is that the filter component size will be reduced that facilitates compact and economical power electronic system and also the fundamental component can be completely transferred to the output load. It is observed from the table I that by increasing the parameter P from 36 to 54, the input power factor of the converter can be increased and THD of source current can be reduced with the variation of K from 0.4 to 0.9. The simulation of the three phase AC buck converter is analyzed without any filter element at both input side and output side of the converter. It is observed that, the power quality can be improved with higher switching frequency with inclusion of small filter component both at input and output side of the converter circuit for best performance.

VI. CONCLUSION

A three phase bidirectional AC buck converter circuit using power MOSFET operating in high frequency chopping mode is simulated and analysed for parameters that includes input power factor, harmonic profile and efficiency of the converter fed to the R load. The EPWM technique is a method where number of pulses per half cycle (P) is increased in order to improve the input power factor and harmonic profile. It is observed from the simulation results that the proposed scheme using EPWM technique improves input power factor, reduces low order harmonics, eliminates certain harmonics for certain values of P and hence significantly reduces the filter size of the converter that facilitates compact and economical power electronic converter system.

ACKNOWLEDGMENT

The authors acknowledge the financial support of the Visvesvaraya Technological University, Belgaum sanctioned under VTU research grants. The authors wish to thank BNM Institute of Technology, Bangalore & its R&D centre in Electrical & Electronics Department for providing lab facility in simulating and analyzing harmonic profile, input power factor and efficiency of the proposed three phase bidirectional Buck AC converter in MATLAB/simulink for power quality improvement.

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